GENERAL DESCRIPTION

The CM6800/1 is a controller for power factor corrected, switched mode power suppliers. Power Factor Correction (PFC) allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully compiles with IEC-1000-3-2 specifications. Intended as a BiCMOS version of the industry-standard ML4824, CM6800/1 includes circuits for the implementation of leading edge, average current, "boost" type power factor correction and a trailing edge, pulse width modulator (PWM). Gate-driver with 1A capabilities minimizes the need for external driver circuits. Low power requirements improve efficiency and reduce component costs.

An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current or voltage mode, at up to 250kHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

The only difference between CM6800 and CM6801 is that CM6800 includes an additional folded-back current limit for PWM section to provide short circuit protection function.

FEATURES

- Patent Number #5,565,761, #5,747,977, #5,742,151, #5,804,950, #5,798,635
- Pin to pin compatible with ML4800 and FAN6800
- Additional folded-back current limit for PWM section.
- 23V Bi-CMOS process
- VIN OK guaranteed turn on PWM at 2.5V instead of 1.5V
- Internally synchronized leading edge PFC and trailing edge PWM in one IC
- Slew rate enhanced transconductance error amplifier for ultra-fast PFC response
- Low start-up current (100 μA typ.)
- Low operating current (3.0mA type.)
- Low total harmonic distortion, high PF
- Reduces ripple current in the storage capacitor between the PFC and PWM sections
- Average current, continuous or discontinuous boost leading edge PFC
- VCC OVP Comparator, Low Power Detect Comparator
- PWM configurable for current mode or voltage mode operation
- Current fed gain modulator for improved noise immunity
- Brown-out control, over-voltage protection, UVLO, and soft start, and Reference OK

APPLICATIONS

- Desktop PC Power Supply
- Internet Server Power Supply
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

PIN CONFIGURATION

SOP-16 (S16) / PDIP-16 (P16)
Top View

Pin	Name	Name	Pin
1	IEAO	VEAO	16
2	IAC	VFB	15
3	ISENSE	VREF	14
4	VRMS	VCC	13
5	SS	PFC OUT	12
6	VDC	PWM OUT	11
7	RAMP1	GND	10
8	RAMP2	DC ILIMIT	9

PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	IEAO	PFC transconductance current error amplifier output	0		4.25	V
2	I_{AC}	PFC gain control reference input	0		1	mA
3	I_{SENSE}	Current sense input to the PFC current limit comparator	-5		0.7	V
4	V_{RMS}	Input for PFC RMS line voltage compensation	0		6	V
5	SS	Connection point for the PWM soft start capacitor	0		8	V
6	V_{DC}	PWM voltage feedback input	0		8	V
7	RAMP 1 (RTCT)	Oscillator timing node; timing set by RT CT	1.2		3.9	V
8	RAMP 2 (PWM RAMP)	When in current mode, this pin functions as the current sense input; when in voltage mode, it is the PWM input from PFC output (feed forward ramp).	0		6	V
9	DC I_{LIMIT}	PWM current limit comparator input	0		1	V
10	GND	Ground				
11	PWM OUT	PWM driver output	0		VCC	V
12	PFC OUT	PFC driver output	0		VCC	V
13	V_{CC}	Positive supply	10	15	18	V
14	V_{REF}	Buffered output for the internal 7.5V reference		7.5		V
15	V_{FB}	PFC transconductance voltage error amplifier input	0	2.5	3	V
16	VEAO	PFC transconductance voltage error amplifier output	0		6	V

BLOCK DIAGRAM (CM6800)

16
VEAO
1
IEAO
13
VCC
VCC
VCC OVP
PFC OVP
7.5V
REFERENCE
VREF
14
0.3V
17.9V
2.75V
LOW POWER
DETECT
TRI-FAULT
0.5V
POWER
FACTOR
CORRECTOR
15
VFB
GMv
3.5K
GMi
2.5V
PFC CMP
S Q
R Q
MPPFC
VCC
IAC
2
GAIN
MODULATOR
-1V
PFC OUT
12
VRMS
4
PFC ILIMIT
3.5K
MNPFC
ISENSE
3
GND
RAMP1
7
OSCILLATOR
CLK
350
PFCOUT
PWM
DUTY
RAMP2
8
SW SPST
DUTY CYCLE
LIMIT
PWMOUT
PWM
CMP
VCC
1.5V
MPPWM
PWM OUT
VDC
6
Vcc
SS CMP
20uA
350
VFB
11
SS
5
MNPWM
1.0V
2.45V
VIN OK
GND
SW SPST
SW SPST
SW SPST
DC ILIMIT
VREF
PULSE
WIDTH
MODULATOR
Q S
VCC
UVLO
DC ILIMIT
9
R
GND
10

BLOCK DIAGRAM (CM6801)

ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6800IP	-40°C to 125°C	16-Pin PDIP (P16)
CM6800IS	-40°C to 125°C	16-Pin Wide SOP (S16)
CM6801IP	-40°C to 125°C	16-Pin PDIP (P16)
CM6801IS	-40°C to 125°C	16-Pin Wide SOP (S16)
CM6800GIP*	-40°C to 125°C	16-Pin PDIP (P16)
CM6800GIS*	-40°C to 125°C	16-Pin Wide SOP (S16)
CM6801GIP*	-40°C to 125°C	16-Pin PDIP (P16)
CM6801GIS*	-40°C to 125°C	16-Pin Wide SOP (S16)

***Note:** G : Suffix for Pb Free Product

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC}		20	V
IEAO	0	4.5	V
I_{SENSE} Voltage	-5	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
PWMOUT	GND – 0.3	VCC + 0.3	V
Voltage on Any Other Pin	GND – 0.3	VCC + 0.3	V
I_{REF}		10	mA
I_{AC} Input Current		1	mA
Peak PFC OUT Current, Source or Sink		1	A
Peak PWM OUT Current, Source or Sink		1	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 80 105	 ℃/W ℃/W

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc=+15V, R_T = 52.3kΩ, C_T = 470pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6800/1			Unit
			Min.	Typ.	Max.	
Voltage Error Amplifier (g_{mv})						
	Input Voltage Range		0		6	V
	Transconductance	$V_{NONINV} = V_{INV}$, VEAO = 3.75V	50	70	90	μmho
	Feedback Reference Voltage		2.45	2.5	2.55	V
	Input Bias Current	Note 2	-1.0	-0.05		μA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V_{FB} = 3V, VEAO = 6V		-35	-20	μA
	Source Current	V_{FB} = 1.5V, VEAO = 1.5V	30	40		μA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	50	60		dB
Current Error Amplifier (g_{mi})						
	Input Voltage Range		-1.5		0.7	V
	Transconductance	$V_{NONINV} = V_{INV}$, VEAO = 3.75V	50	85	100	μmho
	Input Offset Voltage		-15		25	mV
	Output High Voltage		4.0	4.25		V
	Output Low Voltage			1.0	1.2	V

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

Vcc=+15V, R_T = 52.3kΩ, C_T = 470pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6800/1 Min.	CM6800/1 Typ.	CM6800/1 Max.	Unit
	Sink Current	I_{SENSE} = +0.5V, IEAO = 4.0V		-65	-35	μA
	Source Current	I_{SENSE} = -0.5V, IEAO = 1.5V	35	75		μA
	Open Loop Gain		60	70		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
	PFC OVP Comparator					
	Threshold Voltage		2.70	2.77	2.85	V
	Hysteresis		230		290	mV
	Low Power Detect Comparator					
	Threshold Voltage		0.2	0.3	0.4	V
	VCC OVP Comparator					
	Threshold Voltage		17.5	17.9	18.5	V
	Hysteresis		1.40	1.5	1.65	V
	Tri-Fault Detect					
	Fault Detect HIGH		2.65	2.75	2.85	V
	Time to Fault Detect HIGH	V_{FB}=$V_{FAULT\ DETECT\ LOW}$ to V_{FB}=OPEN.470pF from V_{FB} to GND		2	4	ms
	Fault Detect LOW		0.4	0.5	0.6	V
	PFC I_{LIMIT} Comparator					
	Threshold Voltage		-1.10	-1.00	-0.90	V
	(PFC I_{LIMIT} V_{TH} – Gain Modulator Output)		20	100		mV
	Delay to Output (Note 4)	Overdrive Voltage = -100mV		250		ns
	DC I_{LIMIT} Comparator					
	Threshold Voltage		0.95	1.0	1.05	V
	Delay to Output (Note 4)	Overdrive Voltage = 100mV		250		ns
	V_{IN} OK Comparator					
	OK Threshold Voltage		2.35	2.45	2.55	V
	Hysteresis		0.95	1.2	1.4	V
	GAIN Modulator					
	Gain (Note 3)	I_{AC} = 100μA, V_{RMS} =0, V_{FB} = 1V	0.70	0.84	0.95	
		I_{AC} = 100μA, V_{RMS} = 1.1V, V_{FB} = 1V	1.80	2.00	2.20	
		I_{AC} = 150μA, V_{RMS} = 1.8V, V_{FB} = 1V	0.90	1.00	1.10	
		I_{AC} = 300μA, V_{RMS} = 3.3V, V_{FB} = 1V	0.25	0.32	0.40	
	Bandwidth	I_{AC} = 100μA		10		MHz
	Output Voltage = 3.5K*(I_{SENSE}-I_{OFFSET})	I_{AC} = 250μA, V_{RMS} = 1.1V, V_{FB} = 1V	0.84	0.90	0.95	V
	Oscillator					
	Initial Accuracy	T_A = 25℃	66		76	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	68		84	kHz
	Ramp Valley to Peak Voltage			2.5		V
	PFC Dead Time (Note 4)		600		860	ns
	CT Discharge Current	V_{RAMP2} = 0V, V_{RAMP1} = 2.5V	6.5		15	mA

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

Vcc=+15V, R_T = 52.3kΩ, C_T = 470pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6800/1			Unit
			Min.	Typ.	Max.	
Reference						
	Output Voltage	T_A = 25℃, I(V_{REF}) = 1mA	7.4	7.5	7.6	V
	Line Regulation	11V < V_{CC} < 16.5V		10	25	mV
	Load Regulation	0mA < I(V_{REF}) < 7mA; T_A = 0℃~70℃		10	20	mV
		0mA < I(V_{REF}) < 5mA; T_A = -40℃~85℃		10	20	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.35		7.65	V
	Long Term Stability	T_J = 125℃, 1000HRs	5		25	mV
PFC						
	Minimum Duty Cycle	V_{IEAO} > 4.0V			0	%
	Maximum Duty Cycle	V_{IEAO} < 1.2V	92	95		%
	Output Low Rdson	I_{OUT} = -20mA at room temp			15	ohm
		I_{OUT} = -100mA at room temp			15	ohm
		I_{OUT} = 10mA, V_{CC} = 9V at room temp		0.4	0.8	V
	Output High Rdson	I_{OUT} = 20mA at room temp		15	20	ohm
		I_{OUT} = 100mA at room temp		15	20	ohm
	Rise/Fall Time (Note 4)	C_L = 1000pF		50		ns
PWM						
	Duty Cycle Range		0-44	0-47	0-49	%
	Output Low Rdson	I_{OUT} = -20mA at room temp			15	ohm
		I_{OUT} = -100mA at room temp			15	ohm
		I_{OUT} = 10mA, V_{CC} = 9V		0.4	0.8	V
	Output High Rdson	I_{OUT} = 20mA at room temp		15	20	ohm
		I_{OUT} = 100mA at room temp		15	20	ohm
	Rise/Fall Time (Note 4)	C_L = 1000pF		50		ns
	PWM Comparator Level Shift		1.5	1.7	1.9	V
Supply						
	Start-Up Current	V_{CC} = 12V, C_L = 0		100	150	μA
	Operating Current	14V, C_L = 0		3.0	7.0	mA
	Undervoltage Lockout Threshold	CM6800/1	12.74	13	13.26	V
	Undervoltage Lockout Hysteresis	CM6800/1	2.85	3.0	3.15	V

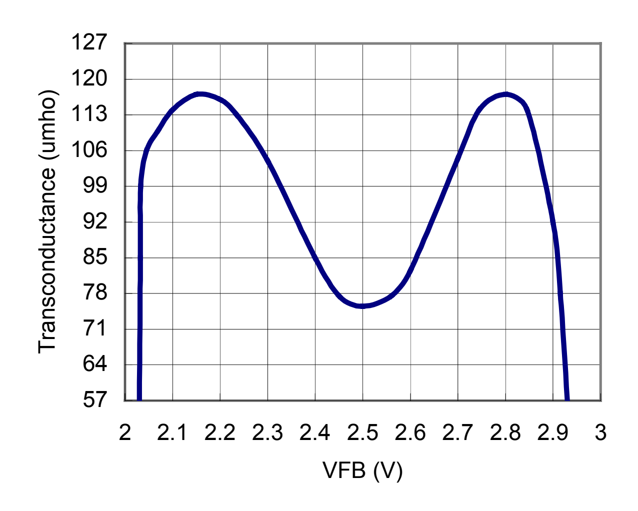
Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V_{FB} pin.

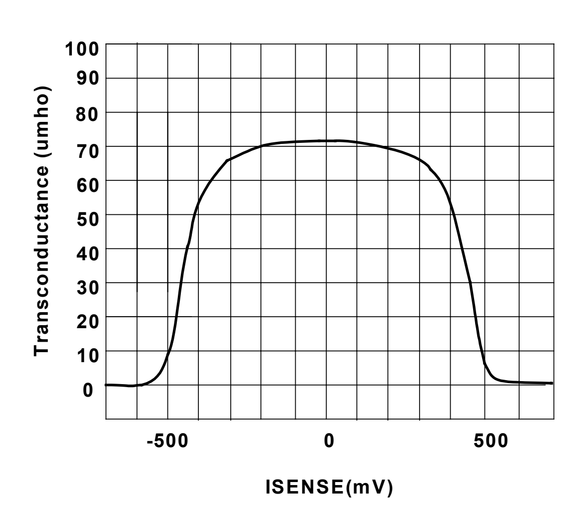
Note 3: Gain = K x 5.375V; K = (I_{SENSE} – I_{OFFSET}) x [I_{AC} (VEAO – 0.625)]$^{-1}$; $VEAO_{MAX}$ = 6V

Note 4: Guaranteed by design, not 100% production test.

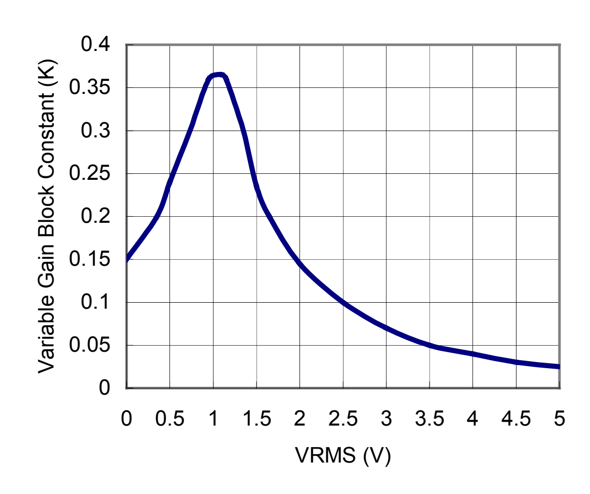
TYPICAL PERFORMANCE CHARACTERISTIC



Voltage Error Amplifier (g_{mv}) Transconductance

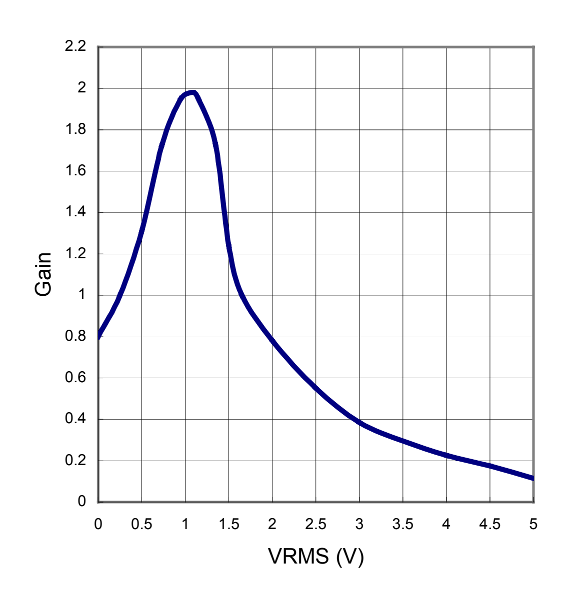


Current Error Amplifier (g_{mi}) Transconductance



Gain Modulator Transfer Characteristic (K)

$$K = \frac{I_{GAINMOD} - I_{OFFSET}}{I_{AC} \text{ x } (6 - 0.625)} mV^{-1}$$



Gain

$$Gain = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}}$$

Functional Description

The CM6800/1 consists of an average current controlled, continuous boost Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feedforward from the PFC output buss can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing edge duty cycle modulation, while the PFC uses leading edge modulation. This patented leading/trailing edge modulation technique results in a higher usable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronized of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the CM6800/1 runs at the same frequency as the PFC.

In addition to power factor correction, a number of protection features have been built into the CM6800/1. These include soft-start, PFC overvoltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6800/1 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to 1/VIN2, which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CM6800/1 PFC is of the current-averaging type, no slope compensation is required.

PFC Section

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the CM6800/1. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and waveshape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The gain modulator's output is inversely proportional to V_{RMS}^2 (except at unusually low values of V_{RMS} where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is called K, and is illustrated in the Typical Performance Characteristics.
3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC form the power line. The general for of the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times VEAO}{V_{RMS}^{2}} \times 1V \qquad (1)$$

More exactly, the output current of the gain modulator is given by:

$I_{GAINMOD}$ = K x (VEAO – 0.625V) x I_{AC}

Where K is in units of V^{-1}

Note that the output current of the gain modulator is limited around 228.47 μA and the maximum output voltage of the gain modulator is limited to 228.47uA x 3.5K=0.8V. This 0.8V also will determine the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. I_{SENSE} = $I_{GAINMOD}$-I_{OFFSET} and I_{OFFSET} can only be measured when VEAO is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 60uA.

Selecting R_{AC} for IAC pin

IAC pin is the input of the gain modulator. IAC also is a current mirror input and it requires current input. By selecting a proper resistor R_{AC}, it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

R_{AC}=Vin peak x 7.9K. For example, if the minimum line voltage is 80VAC, the R_{AC}=80 x 1.414 x 7.9K=894Kohm.

Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin. The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

Cycle-By-Cycle Current Limiter and Selecting R_S

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than –1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_S = $I_{GAINMOD}$ x 3.5K. Since the maximum output voltage of the gain modulator is $I_{GAINMOD}$ max x 3.5K= 0.8V during the steady state, R_S x line input current will be limited below 0.8V as well. Therefore, to choose R_S, we use the following equation:

R_S =0.8V x Vinpeak/(2x Line Input power)

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 200Watt, R_S = (0.8V x 80V x 1.414)/(2 x 200) = 0.226 ohm.

PFC OVP

In the CM6800/1, PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB exceeds 2.75V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below 2.50V. The VFB power components and the CM6800/1 are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop. Also, VCC OVP can be served as a redundant PFCOVP protection. VCC OVP threshold is 17.9V with 1.5V hysteresis.

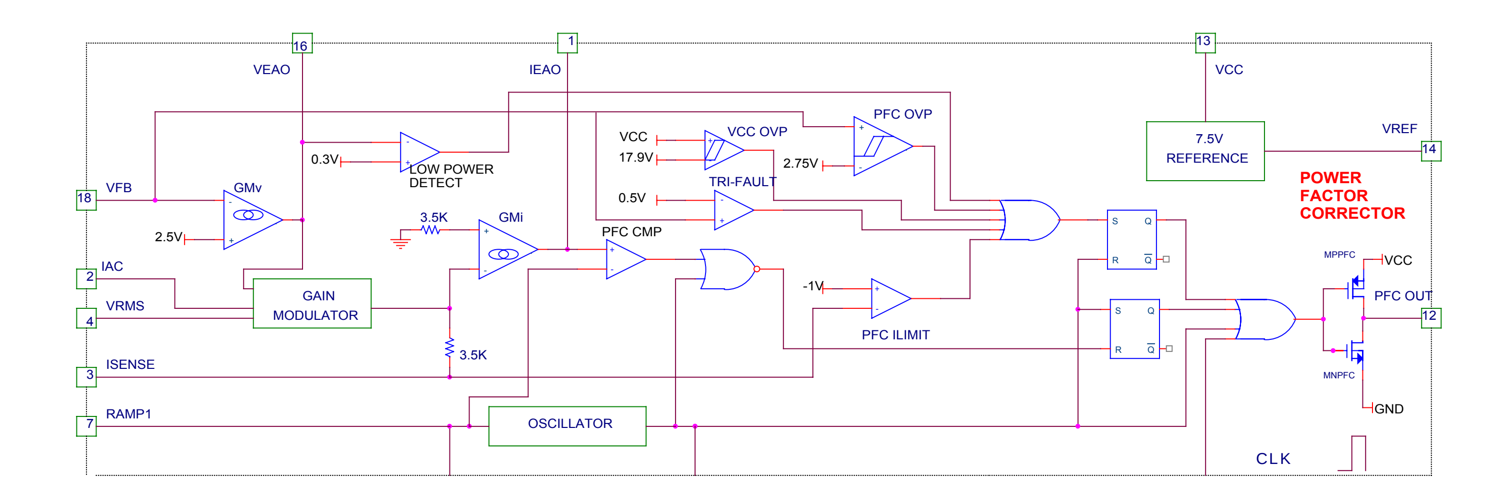


Figure 1. PFC Section Block Diagram

Error Amplifier Compensation
The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on I_{EAO} which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

PFC Voltage Loop
There are two major concerns when compensating the voltage loop error amplifier, V_{EAO}; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the CM6800/1's voltage error amplifier, V_{EAO} has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GM_v: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

PFC Current Loop
The current amplifier, I_{EAO} compensation is similar to that of the voltage error amplifier, V_{EAO} with exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 16.7kHz for a 100kHz switching frequency.

The Current Loop Gain (S)

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}}$$

$$\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI}$$

Z_{CI}: Compensation Net Work for the Current Loop
GM_I: Transconductance of IEAO
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the Z_{CI}
R_S: The Sensing Resistor of the Boost Converter
2.5V: The Amplitude of the PFC Leading Modulation Ramp
L: The Boost Inductor

There is a modest degree of gain contouring applied to the transfer characteristic of the current error amplifier, to increase its speed of response to current-loop perturbations. However, the boost inductor will usually be the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier. This is illustrated in the Typical Performance Characteristics.

I_{SENSE} Filter, the RC filter between R_S and I_{SENSE} :

There are 2 purposes to add a filter at I_{SENSE} pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} Filter to attenuate the energy.
2.) To reduce L, the Boost Inductor: The I_{SENSE} Filter also can reduce the Boost Inductor value since the I_{SENSE} Filter behaves like an integrator before going I_{SENSE} which is the input of the current error amplifier, IEAO.

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm because I_{OFFSET} x the resistor can generate an offset voltage of IEAO. By selecting R_{FILTER} equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 283nF.

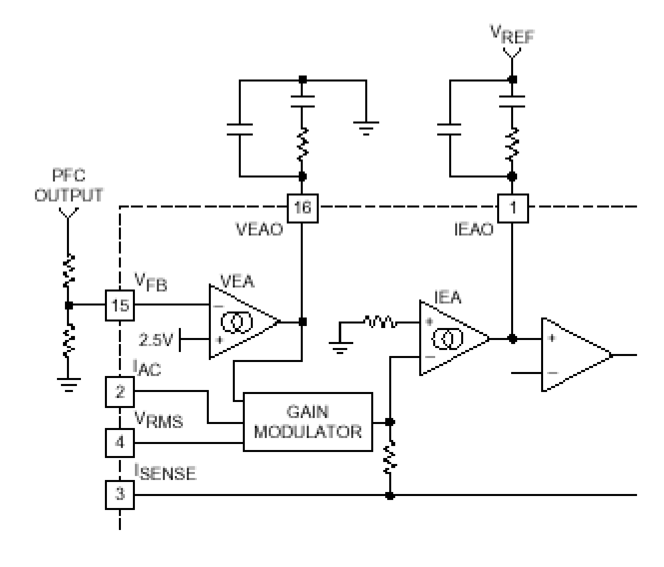


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

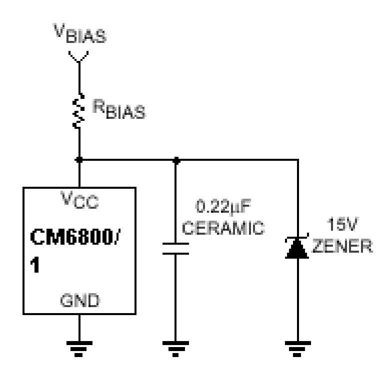


Figure 3. External Component Connections to V_{CC}

Oscillator (RAMP1)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75}$$

at V_{REF} = 7.5V:
$t_{RAMP} = C_T \times R_T \times 0.51$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{5.5mA} \times C_T = 450 \times C_T$$

The dead time is so small ($t_{RAMP} >> t_{DEADTIME}$) that the operating frequency can typically be approximately by:

$$f_{OSC} = \frac{1}{t_{RAMP}}$$

EXAMPLE:
For the application circuit shown in the datasheet, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}}$$

Solving for $C_T \times R_T$ yields 1.96×10^{-5}. Selecting standard components values, C_T = 390pF, and R_T = 51.1kΩ

The dead time of the oscillator adds to the Maximum PWM Duty Cycle (it is an input to the Duty Cycle Limiter). With zero oscillator dead time, the Maximum PWM Duty Cycle is typically 45%. In many applications, care should be taken that C_T not be made so large as to extend the Maximum Duty Cycle beyond 50%. This can be accomplished by using a stable 390pF capacitor for C_T.

PWM Section

Pulse Width Modulator

The PWM section of the CM6800/1 is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DCI_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP2 in such applications. For voltage-mode, operation or certain specialized applications, RAMP2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} will be compared. Under these conditions, the use of voltage feedforward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I_{LIMIT} input is used for output stage overcurrent protection.

No voltage error amplifier is included in the PWM stage of the CM6800/1, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of optocoupler feedback circuitry, an offset has been built into the PWM's RAMP2 input which allows V_{DC} to command a zero percent duty cycle for input voltages below 1.25V.

PWM Current Limit

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. Beside, the cycle-by-cycle current, when the DC ILIMIT triggered the cycle-by-cycle current, it also softly discharge the voltage of soft start capacitor. It will limit PWM duty cycle mode. Therefore, the power dissipation will be reduced during the dead short condition.

V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V_{FB} is less than its nominal 2.45V. Once this voltage reaches 2.45V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

PWM Control (RAMP2)

When the PWM section is used in current mode, RAMP2 is generally used as the sampling point for a voltage representing the current on the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}),that will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feedforward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

Soft Start

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 20μA supplies the charging current for the capacitor, and start-up of the PWM begins at 1.25V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{20\mu A}{1.25V}$$

where C_{SS} is the required soft start capacitance, and the t_{DEALY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS}:

$$C_{SS} = 5ms \times \frac{20\mu A}{1.25V} = 80nF$$

Caution should be exercised when using this minimum soft start capacitance value because premature charging of the SS capacitor and activation of the PWM section can result if VFB is in the hysteresis band of the V_{IN} OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a 1.0 μF soft start capacitor will allow time for V_{FB} and PFC out to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

Generating V_{CC}

After turning on CM6800/1 at 13V, the operating voltage can vary from 10V to 17.9V. The threshold voltage of VCC OVP comparator is 17.9V. The hysteresis of VCC OVP is 1.5V. When VCC see 17.9V, PFCOUT will be low, and PWM section will not be disturbed. That's the two ways to generate VCC. One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias CM6800/1 system. The bootstrap winding can be either taped from PFC boost choke or from the transformer of the DC to DC stage.

The ratio of winding transformer for the bootstrap should be set between 18V and 15V. A filter network is recommended between VCC (pin 13) and bootstrap winding. The resistor of the filter can be set as following.

$R_{FILTER} \times I_{VCC} \sim 2V$, $I_{VCC} = I_{OP} + (Q_{PFCFET} + Q_{PWMFET}) \times fsw$

$I_{OP} = 3mA$ (typ.)

If anything goes wrong, and VCC goes beyond 19.4V, the PFC gate (pin 12) drive goes low and the PWM gate drive (pin 11) remains function. The resistor's value must be chosen to meet the operating current requirement of the CM6800/1 itself (5mA, max.) plus the current required by the two gate driver outputs.

EXAMPLE:

With a wanting voltage called, V_{BIAS} ,of 18V, a VCC of 15V and the CM6800/1 driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA$

$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G}$$

$$R_{BIAS} = \frac{18V - 15V}{5mA + 9mA}$$

Choose $R_{BIAS} = 214\Omega$

The CM6800/1 should be locally bypassed with a 1.0 μF ceramic capacitor. In most applications, an electrolytic capacitor of between 47 μF and 220 μF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

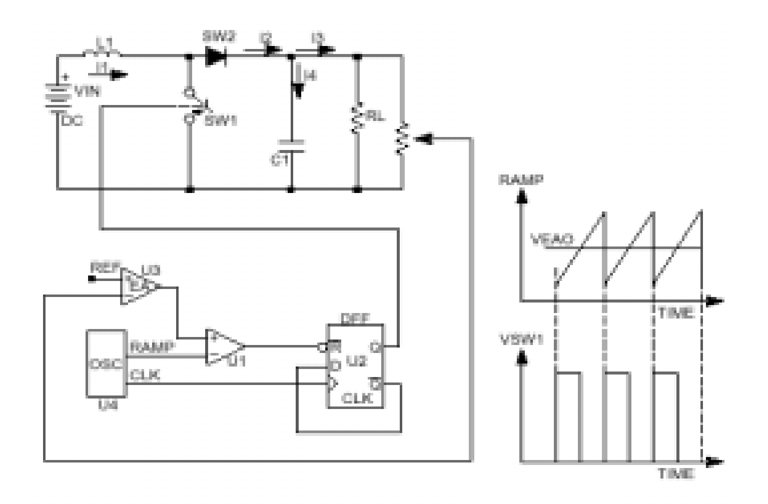


Figure 4. Typical Trailing Edge Control Scheme

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch. Figure 5 shows a leading edge control scheme.

One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

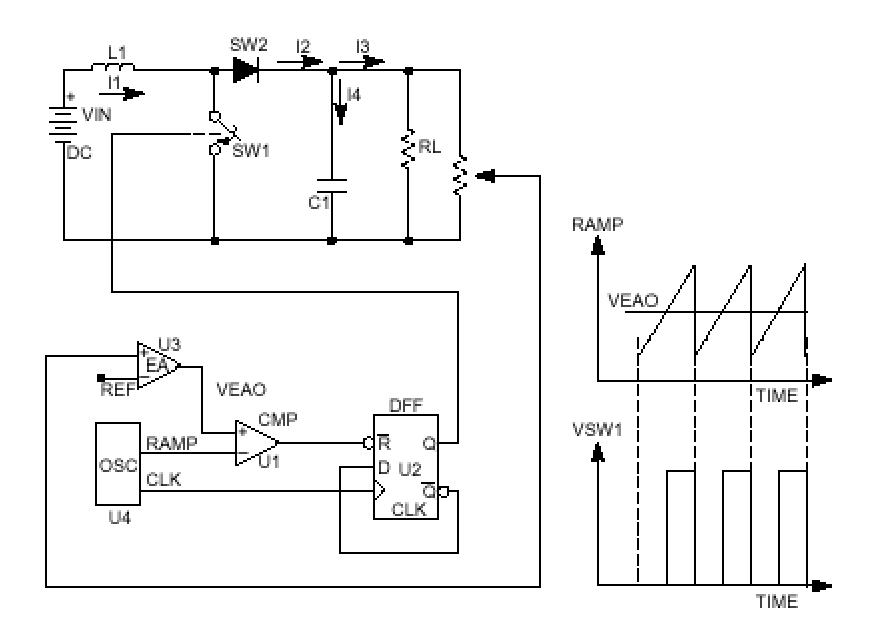


Figure 5. Typical Leading Edge Control Scheme

APPLICATION CIRCUIT (Voltage Mode)

APPLICATION CIRCUIT (Current Mode)

PACKAGE DIMENSION

16-PIN PDIP (P16)

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.32	---	---	0.170
A1	0.38	---	---	0.015	---	---
b	1.40	---	1.65	0.055	---	0.065
b1	0.40	---	0.56	0.016	---	0.022
C	0.20	---	0.31	0.008	---	0.012
D	18.79	---	19.31	0.740	---	0.760
E	7.49	---	8.26	0.295	---	0.325
E1	6.09	---	6.61	0.240	---	0.260
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
m	0.50	---	---	0.02	---	---
θ	0°	---	15°	0°	---	15°

16-PIN SOP (S16), 0.300" Wide Body

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.35	0.089	---	0.093
b	0.35	---	0.51	0.014	---	0.020
C	0.23	---	0.32	0.091	---	0.013
D	10.10	---	10.50	0.398	---	0.413
E	10.00	---	10.65	0.394	---	0.419
E1	7.40	---	7.60	0.291	---	0.299
e	---	1.27	---	---	0.050	---
L	0.40	---	1.27	0.016	---	0.050
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

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